Advanced Digital Receiver for Distributed Instrument Arrays

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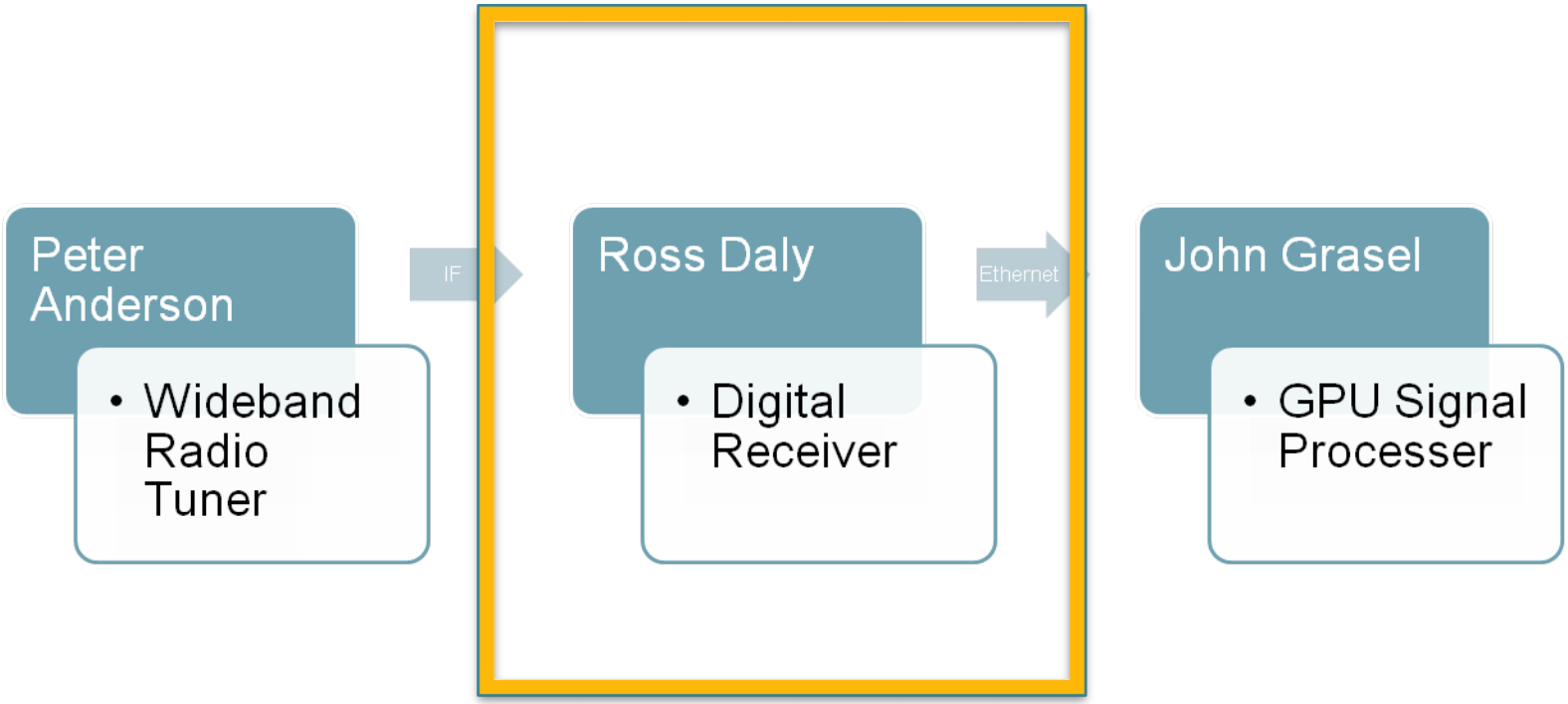
Project Overview

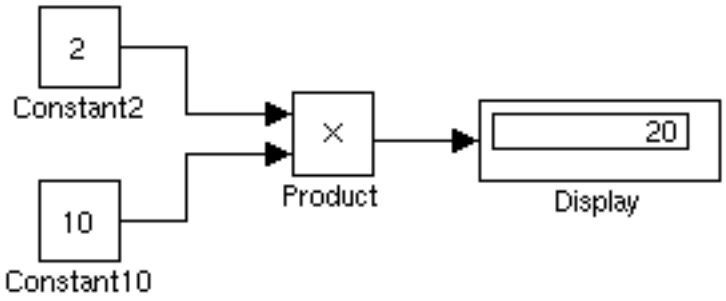


Tools

- Simulink
- System Generator for DSP

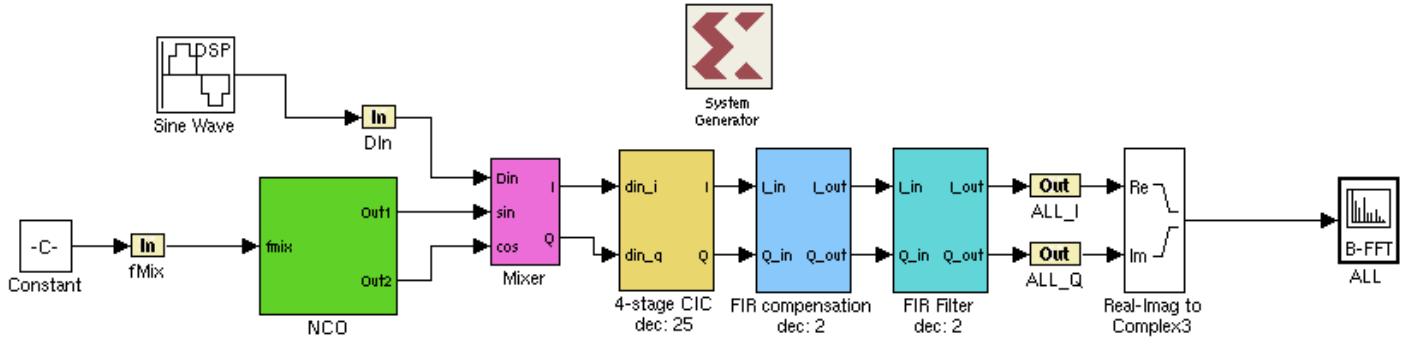
XILINX SYSTEM GENERATOR™ For DSP

MATLAB® SIMULINK®



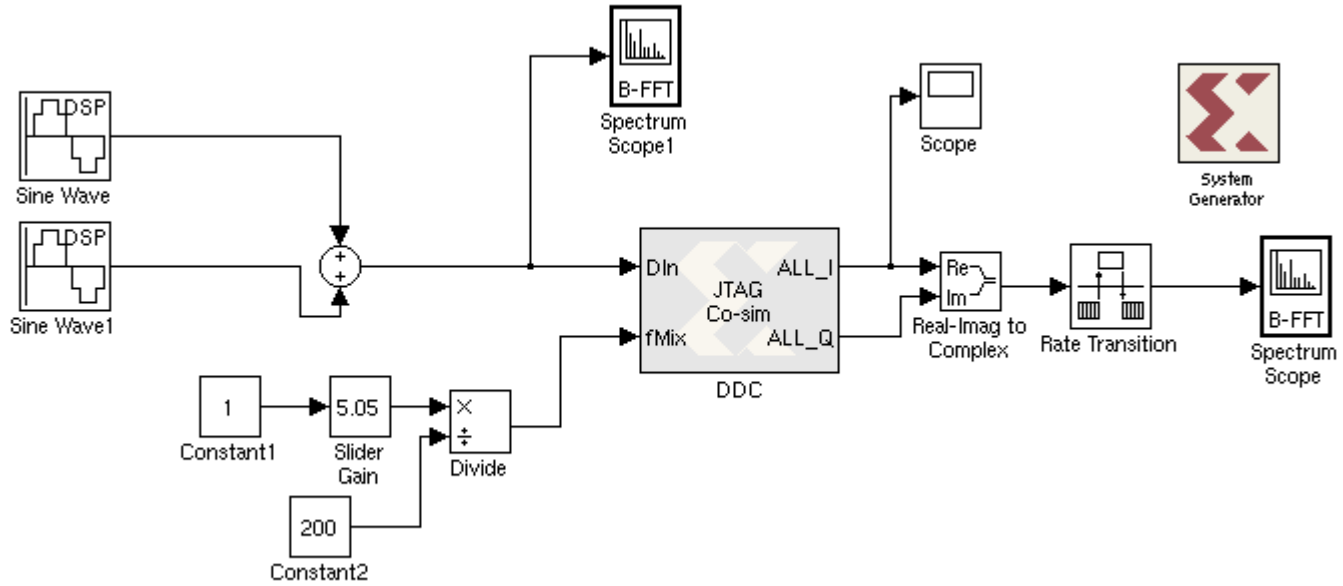
Software Radio Digital Receiver

- Use Programmable Logic (FPGA)
- Digital Down Conversion (DDC)



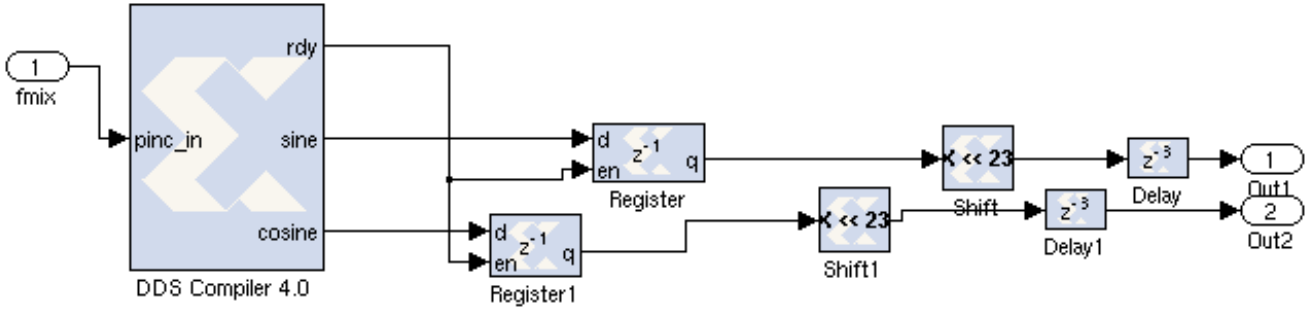
Hardware Co-simulation

- Compile model as Simulink block
- Simulate through Xilinx Chip



Numerically Controlled Oscillator and Mixer

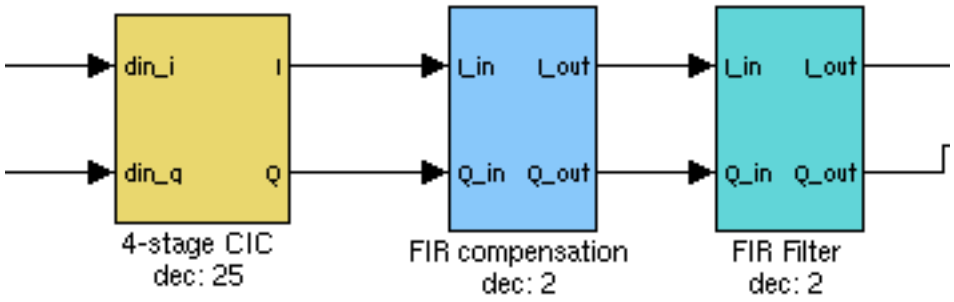
- NCO
- Direct Digital Synthesizer
- Frequency Translation of the Signal



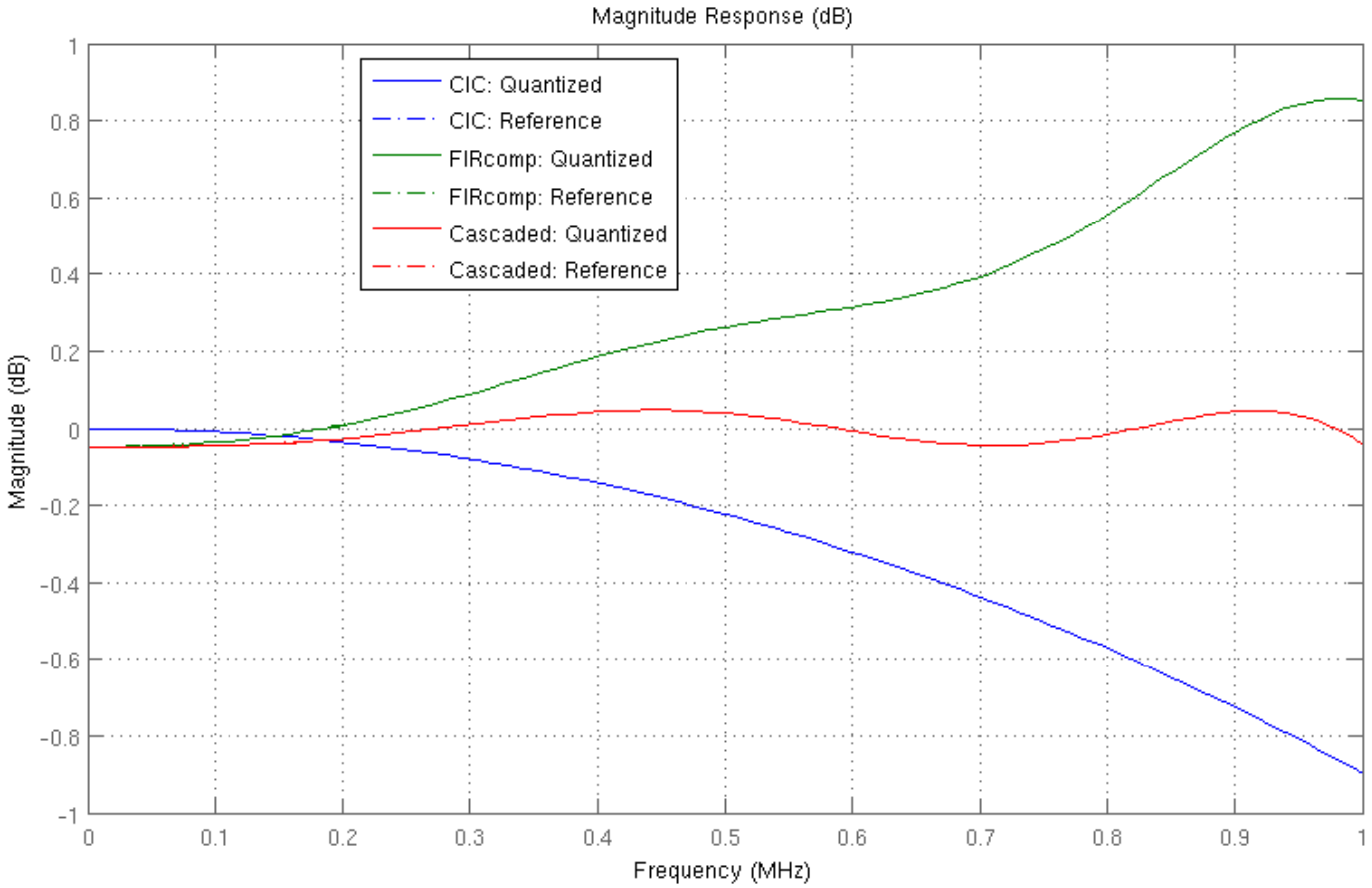
The DDS mixer signal has a spurious free dynamic range (SFDR) of 108 dB

Decimating Filters

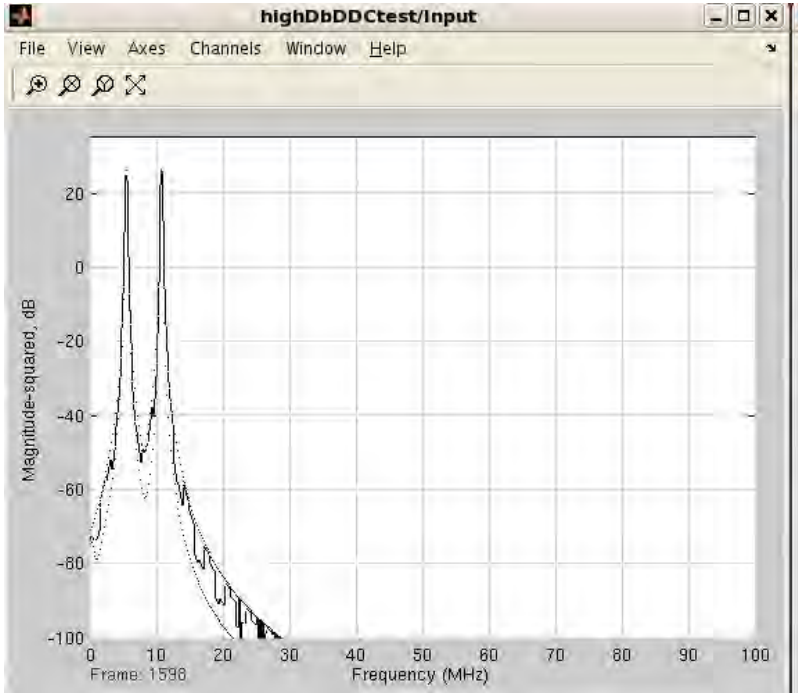
- Cascaded Integrator-Comb (CIC) filter
- Finite Impulse Response (FIR) compensation Filter
- FIR Low Pass filter

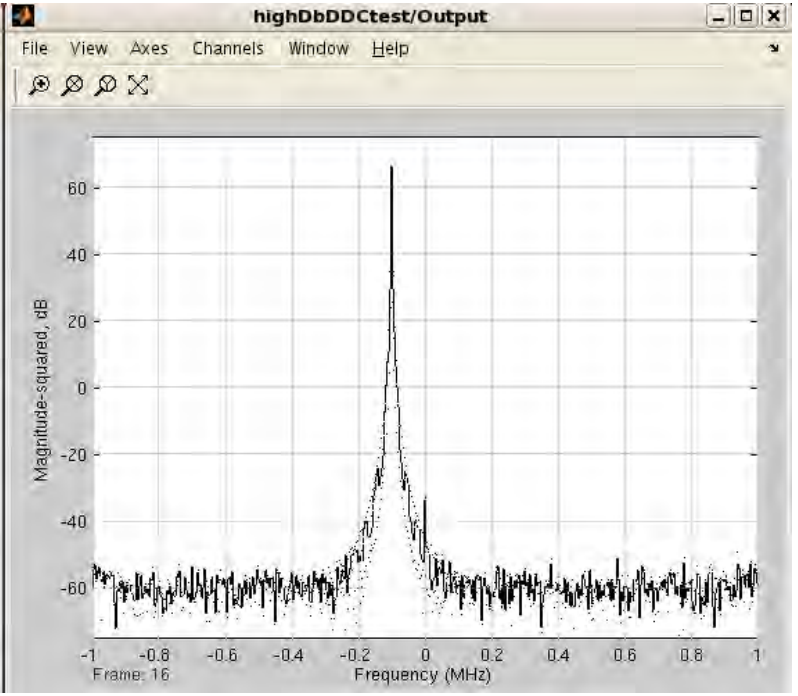


CIC droop correction



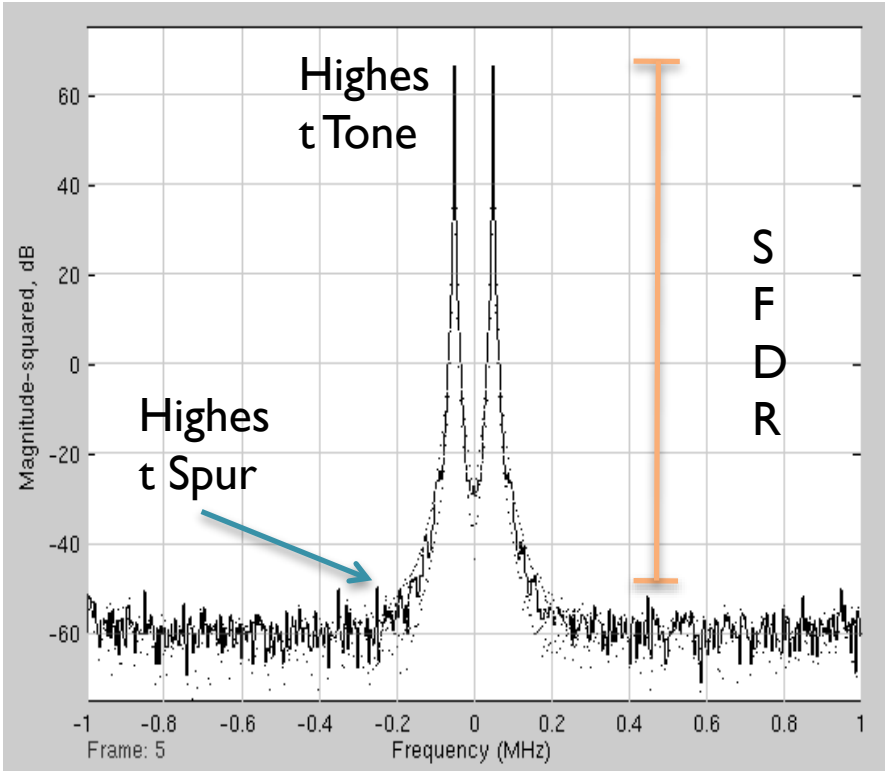
Output of the Digital Down Converter





Results: Spurious Free Dynamic Range (SFDR)

- One Tone and Two Tone SFDR

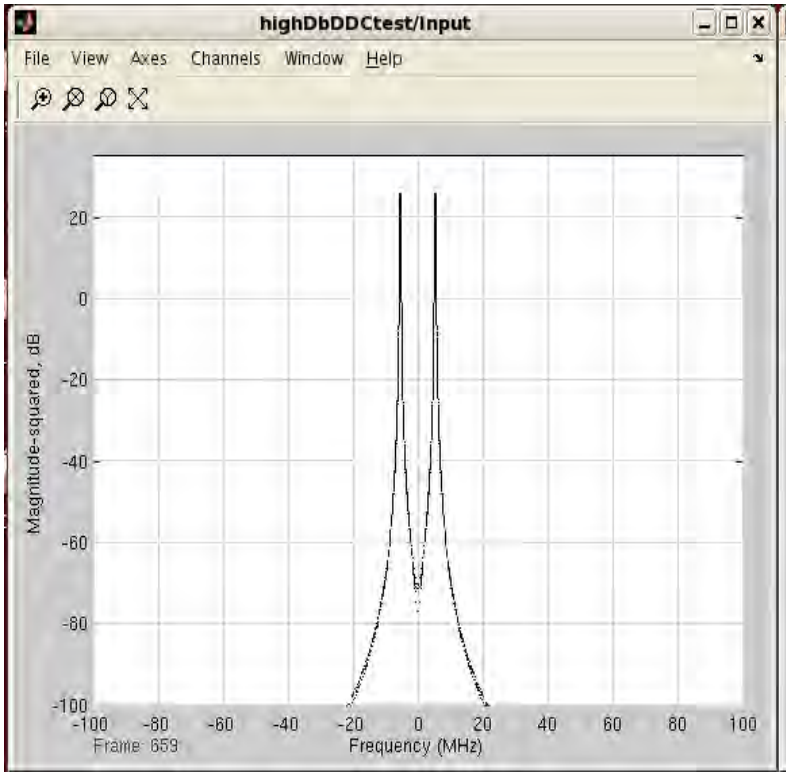


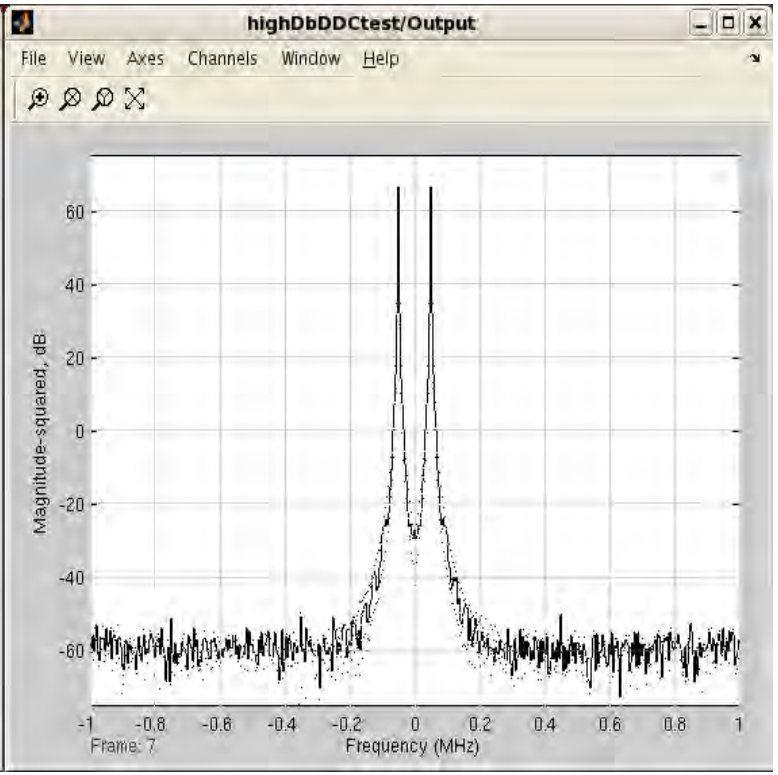
SPURIOUS FREE DYNAMIC RANGE		
Receiver Type	**One Tone**	**Two Tones**
High Dynamic Range	119 dB	114 dB
Low Dynamic Range	98 dB	68 dB

High Dynamic Range

INPUT SIGNAL
200 MHz Sample Rate

OUTPUT OF DDC
2 MHz Sample Rate

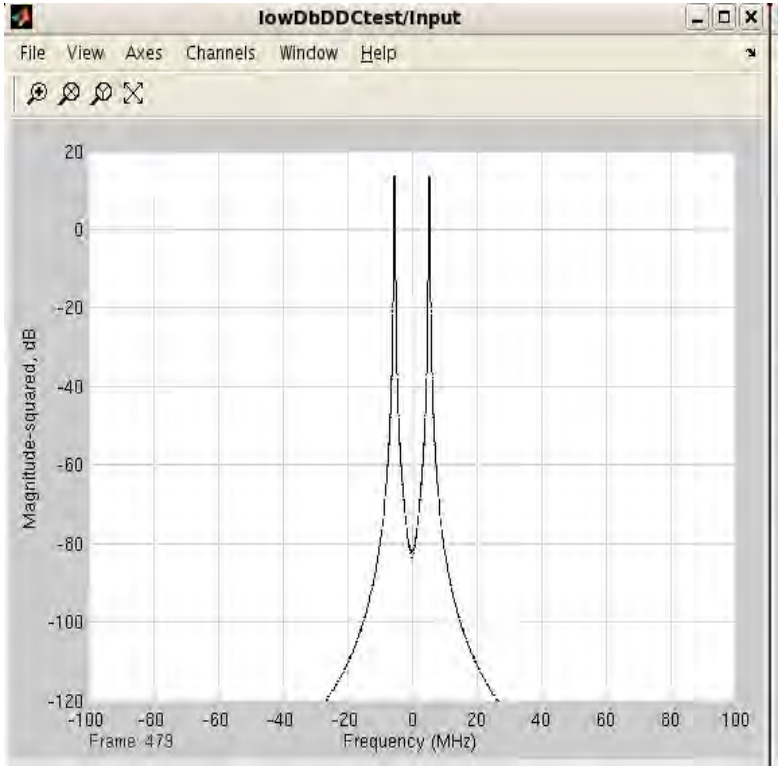


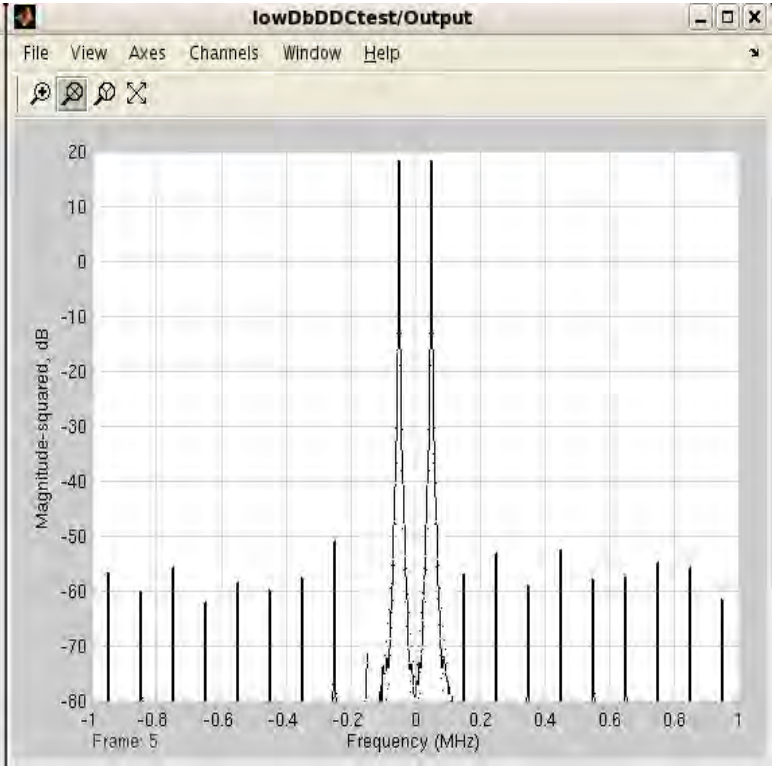


Low Dynamic Range

INPUT SIGNAL
200 MHz Sample Rate

OUTPUT OF DDC
2 MHz Sample Rate



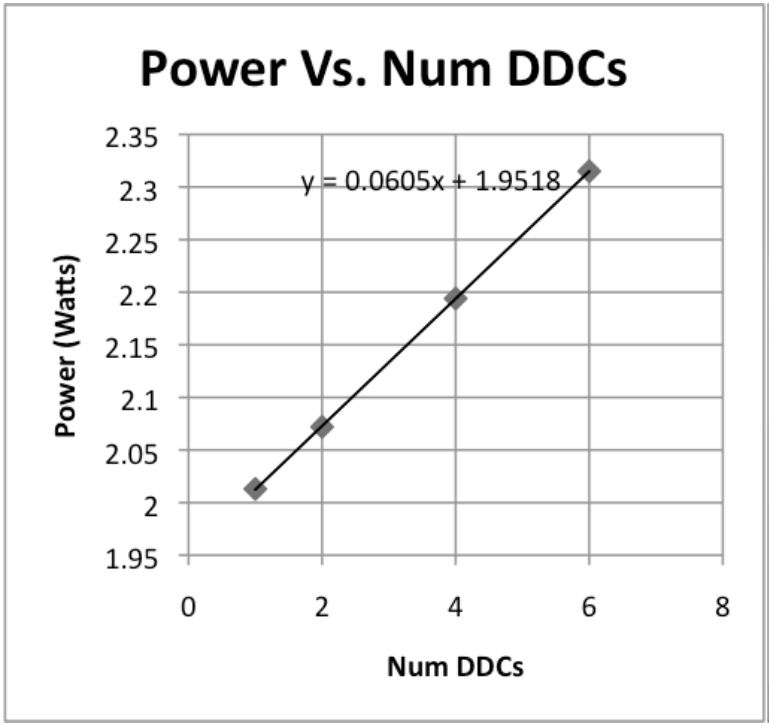


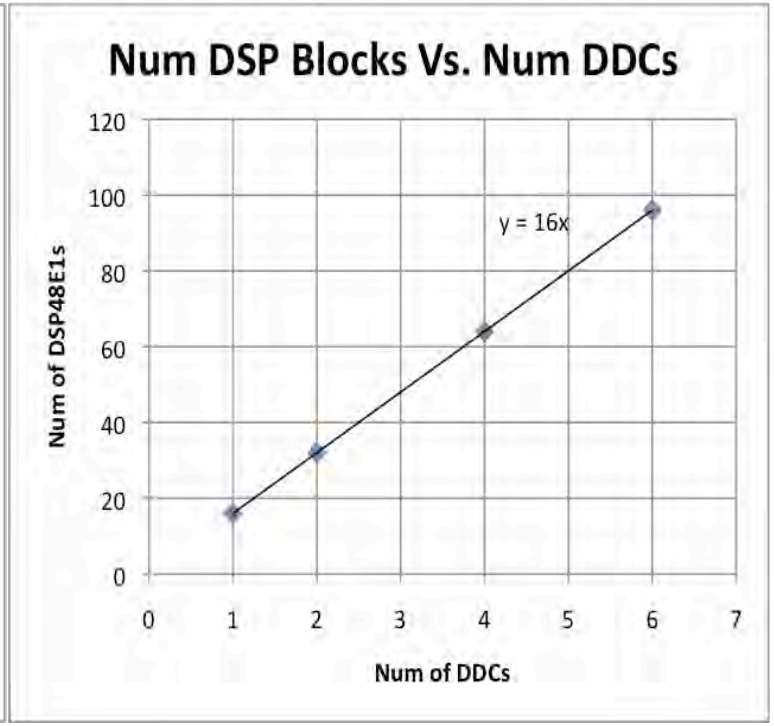
Results: Power Consumption and Hardware Resource Usage

COMPARING TWO DDC DESIGNS		
	High Dynamic Range	Low Dynamic Range
% Registers	<1%	<1%
% Logic Tables	<1%	<1%
% DSP blocks	2.08%	2.08%
Total Power	2.013 Watts	2.010 Watts

- Potential for 48 Digital Down Converters
- Low Dynamic Range Receiver has same resource usage

Hardware Resource Scaling





Future Work

- Analog to Digital Converter Interface
- Ethernet Data Output
- GPS Synchronization Pulse

Experience

- System Generator vs. explicit coding
- Pluses of System Generator
  - Simple in Theory
  - Responsive Technical Support
- Minuses of System Generator
  - Very buggy
  - Need to understand specific details of blocks

Acknowledgements

- Xilinx Tech Support
- My Mentors
- My Peers