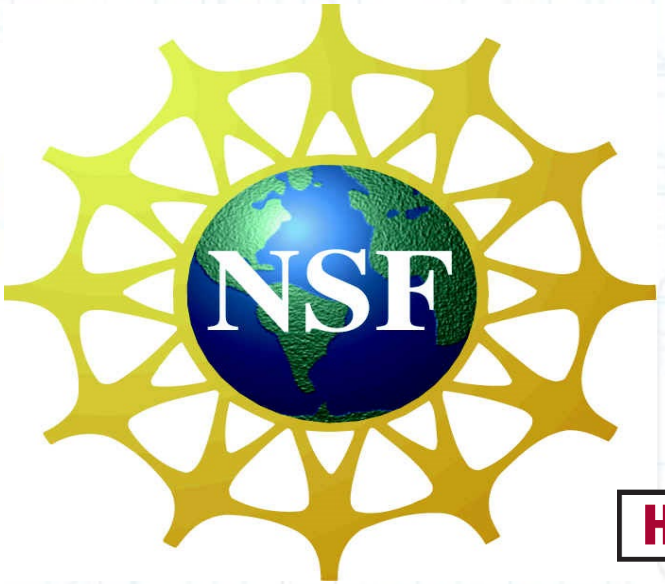
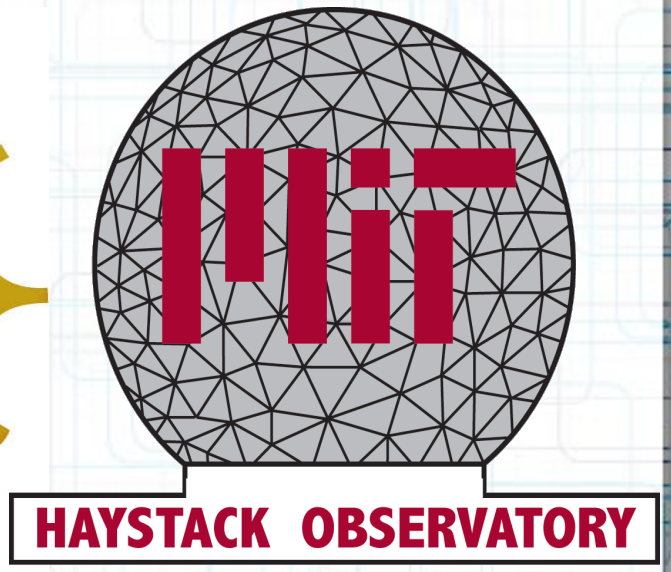
Advanced Digital Receiver for Distributed Instrument Arrays





Patrick Smith – University of Florida

MIT Haystack Observatory REU 2012

Overview

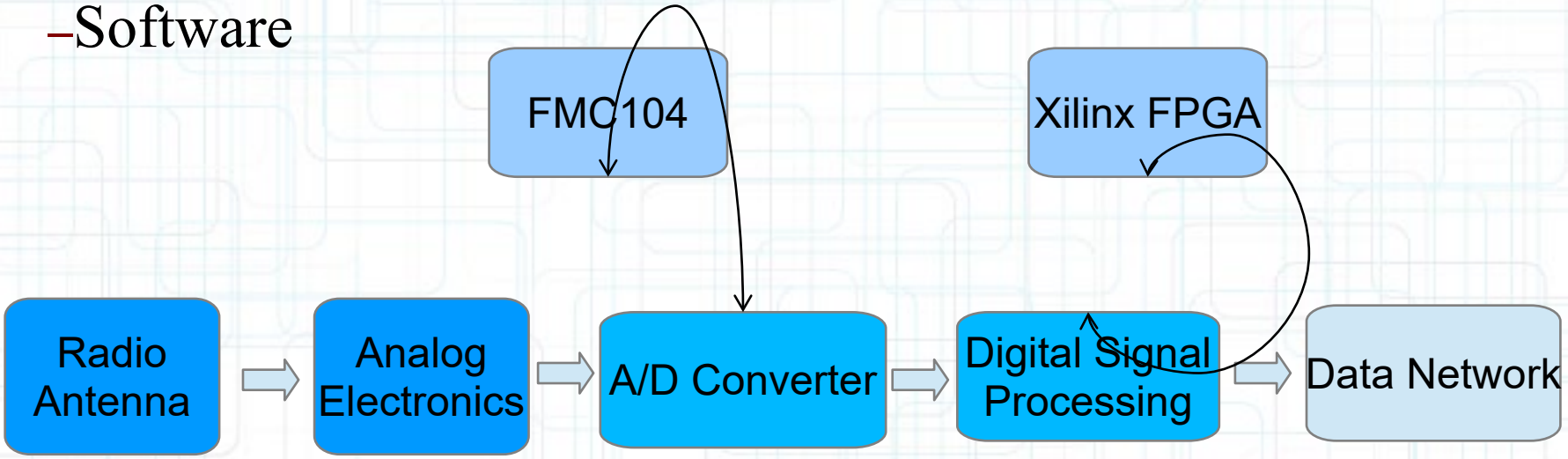
- Goals
- What is a Digital Receiver?
- Hardware
- Development Tools
- Firmware
- Results
- Conclusion

Goals

- Enable next generation of radio signal data acquisition
- Use a commercial 'off the shelf' solution
  - 4DSP FMC104
- Analog to Digital Converter Card
- Interface the 4DSP card with a Xilinx Field Programmable Gate Array (FPGA)
- Develop firmware to implement the interface using a high-level Hardware Description Language (VHDL)

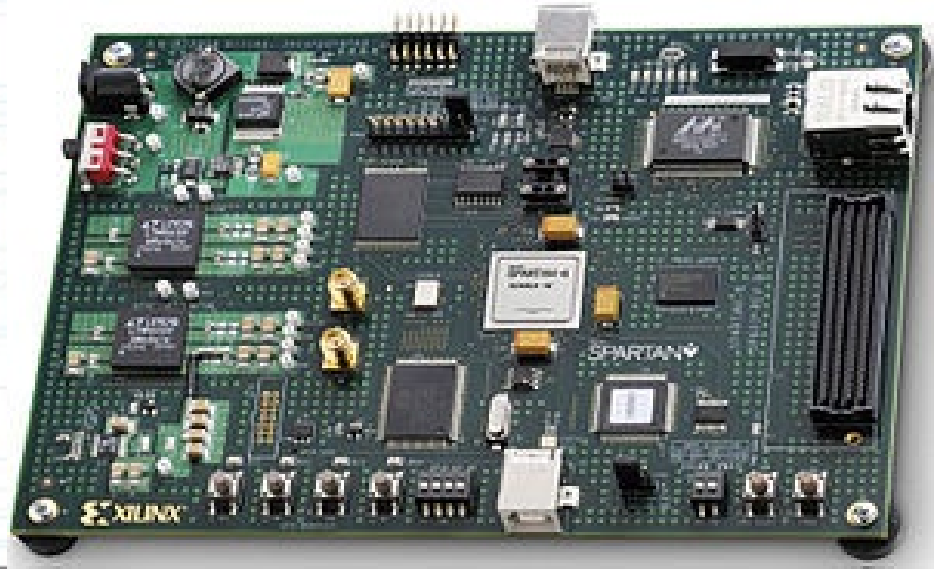
What is a Digital Receiver?

- Radio using Digital Signal Processing
- Eliminate most analog components
- Can be implemented using:
  - Application Specific Integrated Circuit (ASIC)
  - Field Programmable Gate Array
  - Software



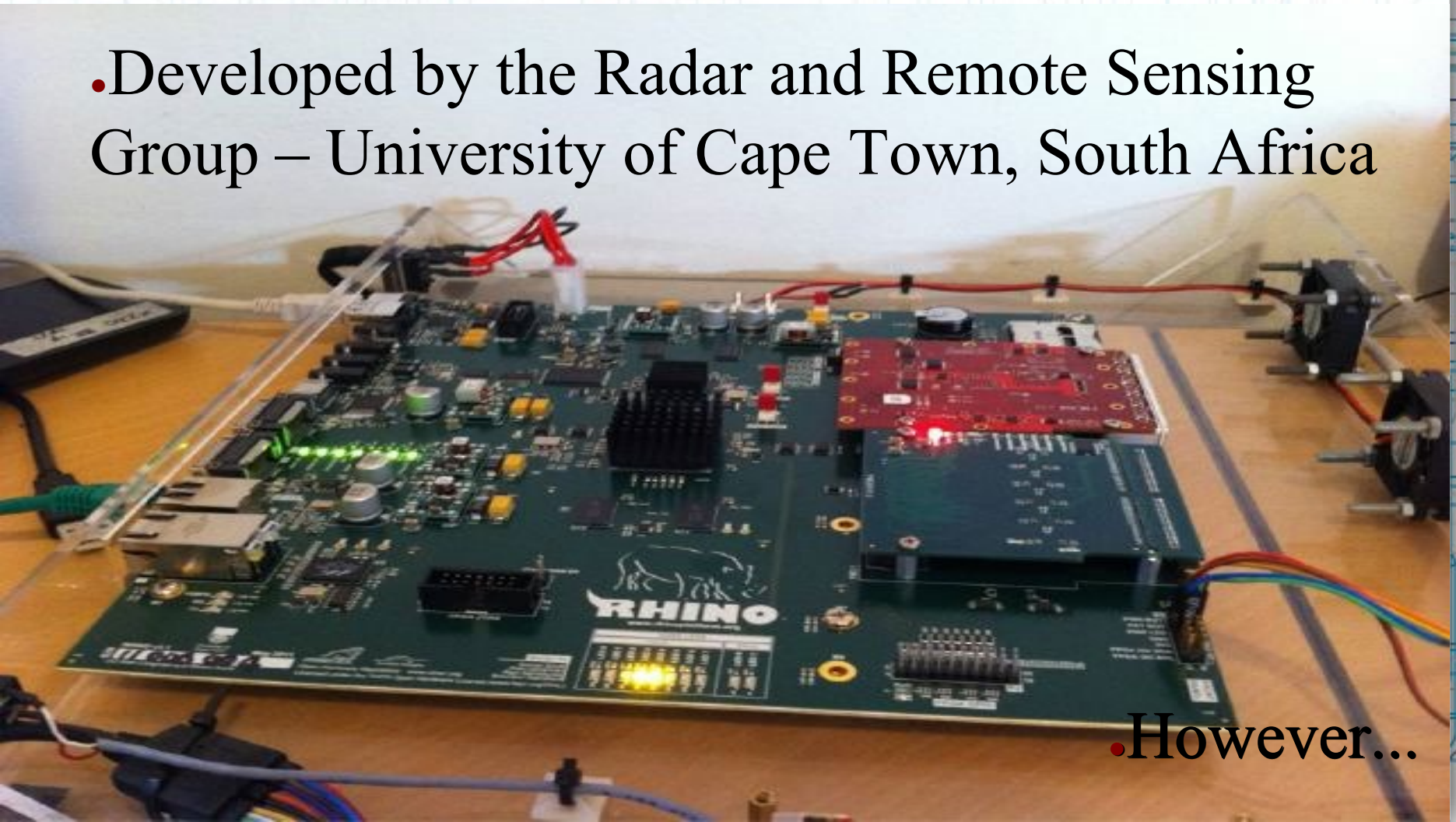
Field Programmable Gate Array (FPGA)

- An FPGA is an integrated circuit that is configured after manufacturing
  - Reconfigurable
- Used in digital interfacing and signal processing
- Modern tools are simplifying a traditionally complex development cycle



FPGA: South African Rhino Board

- Reconfigurable Hardware Interface for Computing and Radio (open source)
- Developed by the Radar and Remote Sensing Group – University of Cape Town, South Africa

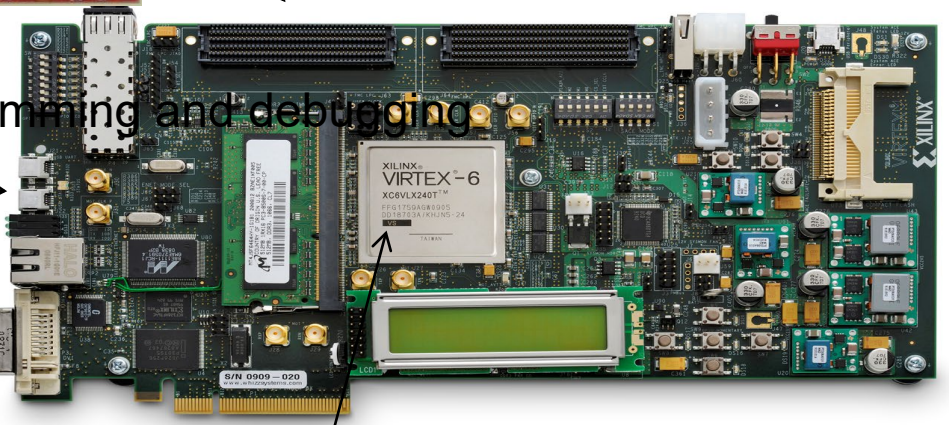


- However...

FPGA: Xilinx Virtex 6 ML605

- Since the Rhino board has been delayed, we turned to the Virtex 6 ML605 board

FPGA Mezzanine Card
Connect analog-to-digital converter card



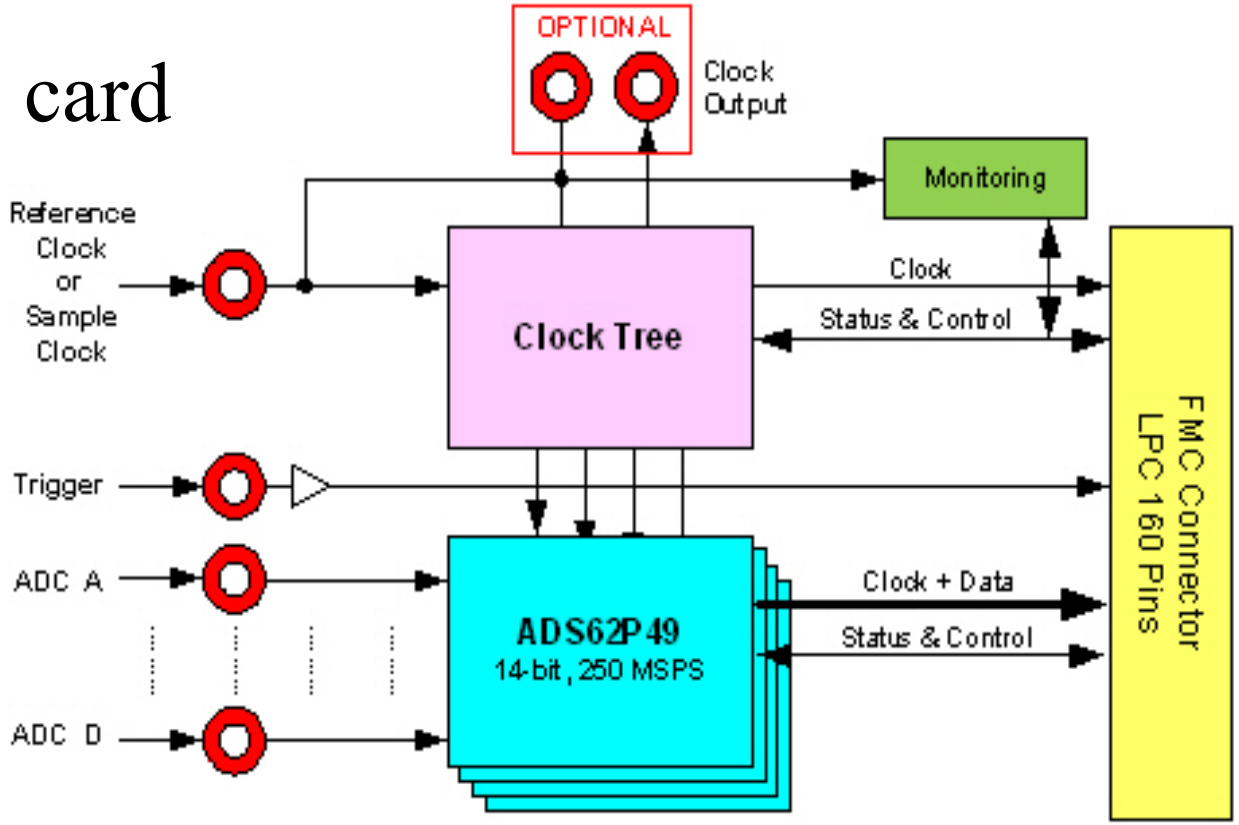
USB
Connect PC for programming and debugging

Ethernet
Transfer data

Xilinx FPGA chip

Analog-to-Digital Conversion

- 4DSP FMC104 ADC card
  - 4 channel
  - 14-bit
  - 250 Msps



- Serial Control
  - Inter-Integrated Circuit (I2C)
- 2 wire bidirectional serial bus
  - Serial Interface for ADC and Clock Control

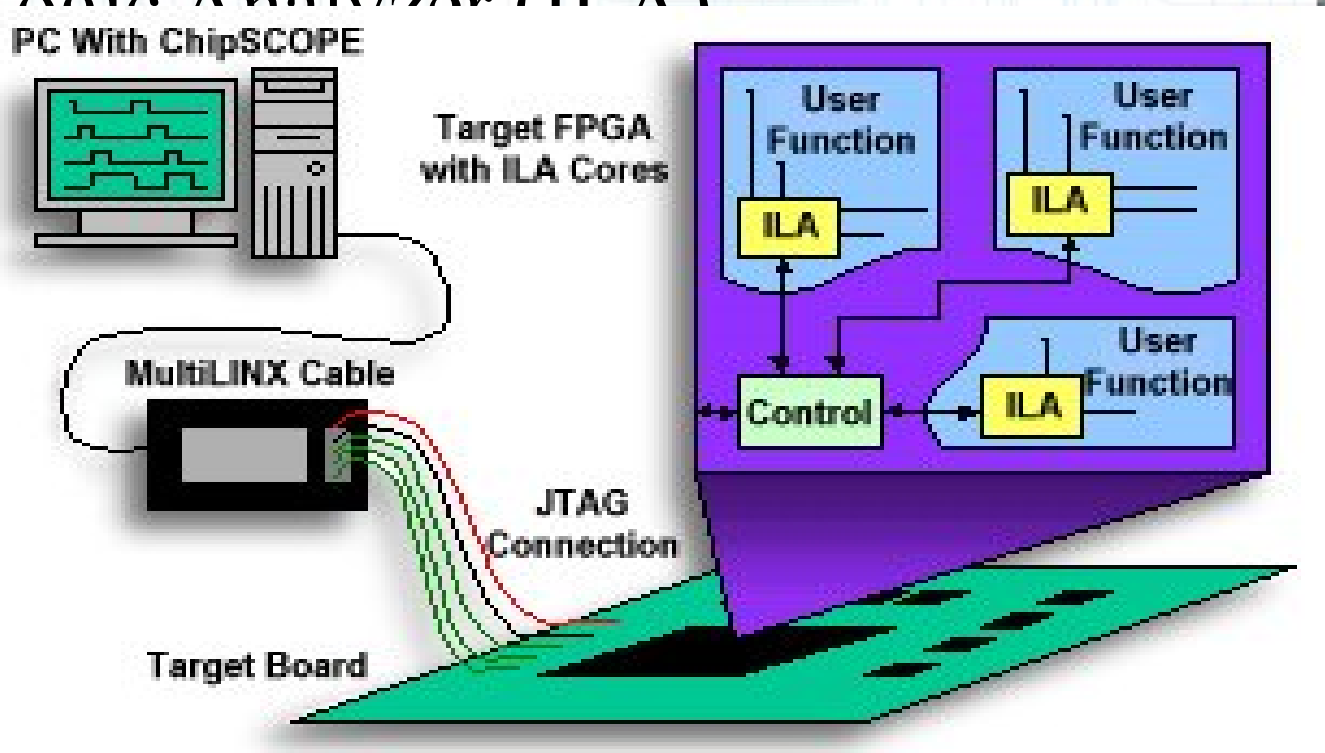
Xilinx Development Tools

- FPGA Development Flow
  - **Synthesis**
- Convert VHDL code to logic gates
  - **Implementation**
- Assign and connect logic resources
  - **Configuration**
- Program the FPGA

```
23  architecture i2c_master_syn of i2c_master is
24  -------------------------------------------------------------------
25  -- Component declarations
26  -------------------------------------------------------------------
27  component wb_i2c_ctrl
28  port (
29    -- Wishbone signals
30    wb_clk_i      : in  std_logic;                     -- master clock input
31    wb_rst_i      : in  std_logic;                     -- synchronous active high reset
32    wb_adr_o      : out std_logic_vector(3 downto 0);  -- lower address bits
33    wb_dat_i      : in  std_logic_vector(7 downto 0);  -- databus input
34    wb_dat_o      : out std_logic_vector(7 downto 0);  -- databus output
35    wb_sel_o      : out std_logic_vector(3 downto 0);  -- byte select inputs
36    wb_we_o       : out std_logic;                     -- write enable input
```

Xilinx Debugging Tools

- ChipScope
  - Integrated CONtroller (ICON)
  - Virtual Inputs/Outputs (VIO)
  - Integrated Logic Analyzer (ILA)

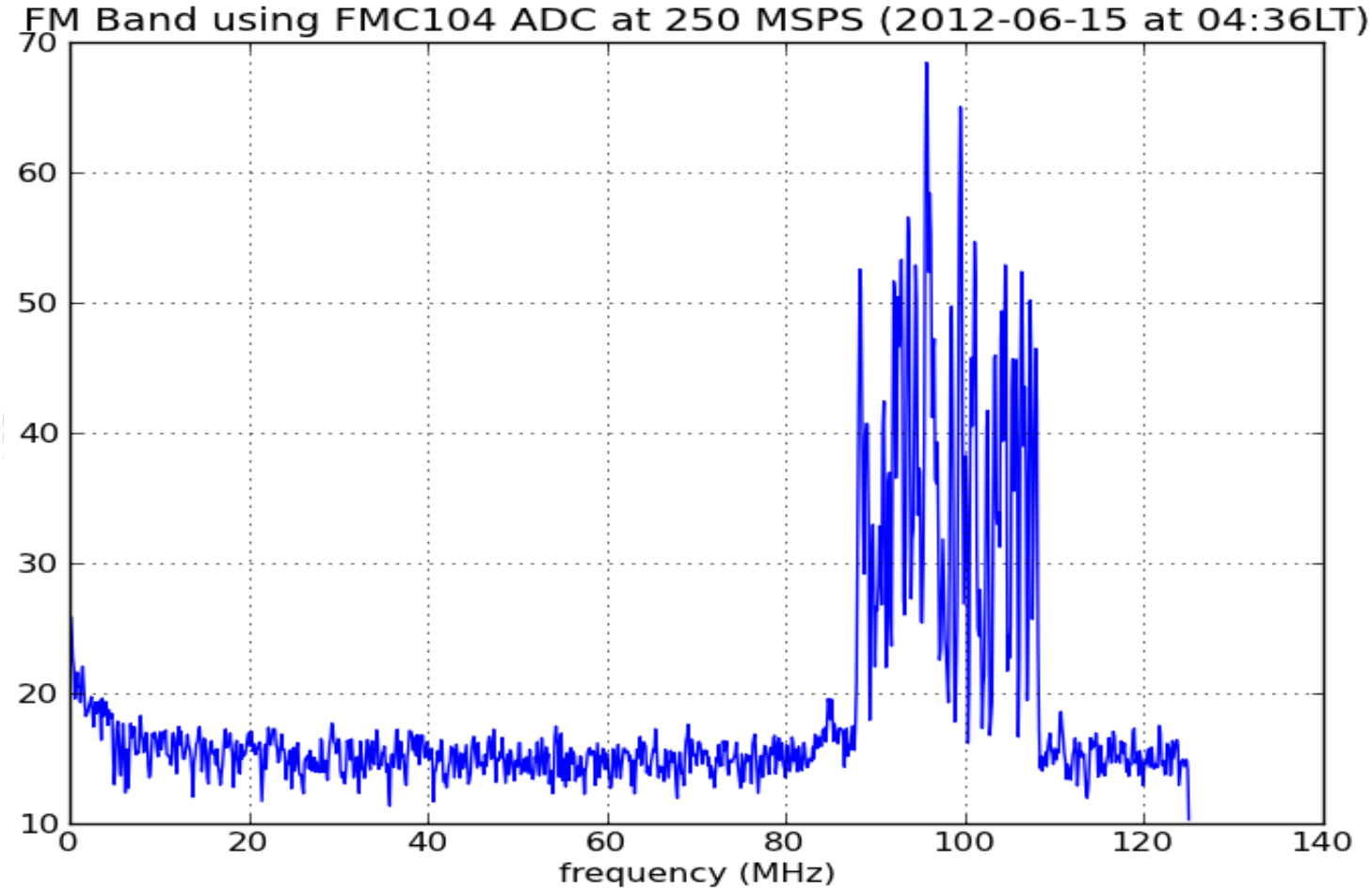


Firmware

- The ADC to FPGA interface logic
  - Enables control of the ADC, Clock Chip, onboard Sensors
  - Interfaces data and transfers it for use
- Ultimately the goal is to transfer data out over ethernet
- The Firmware is complex, need to break into smaller pieces for implementation

Results

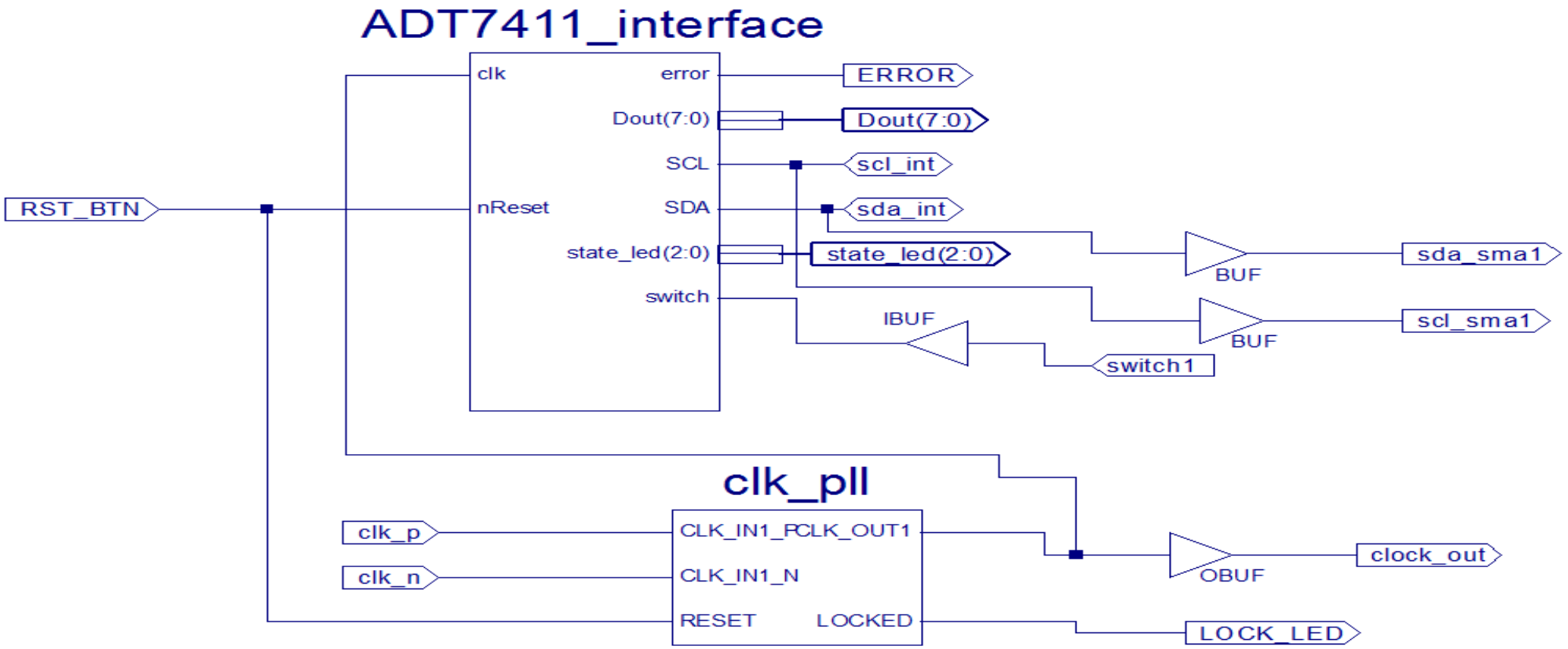
- 4DSP Provided Firmware for Testing



Log Periodic FM radio antenna passed through band-pass filter

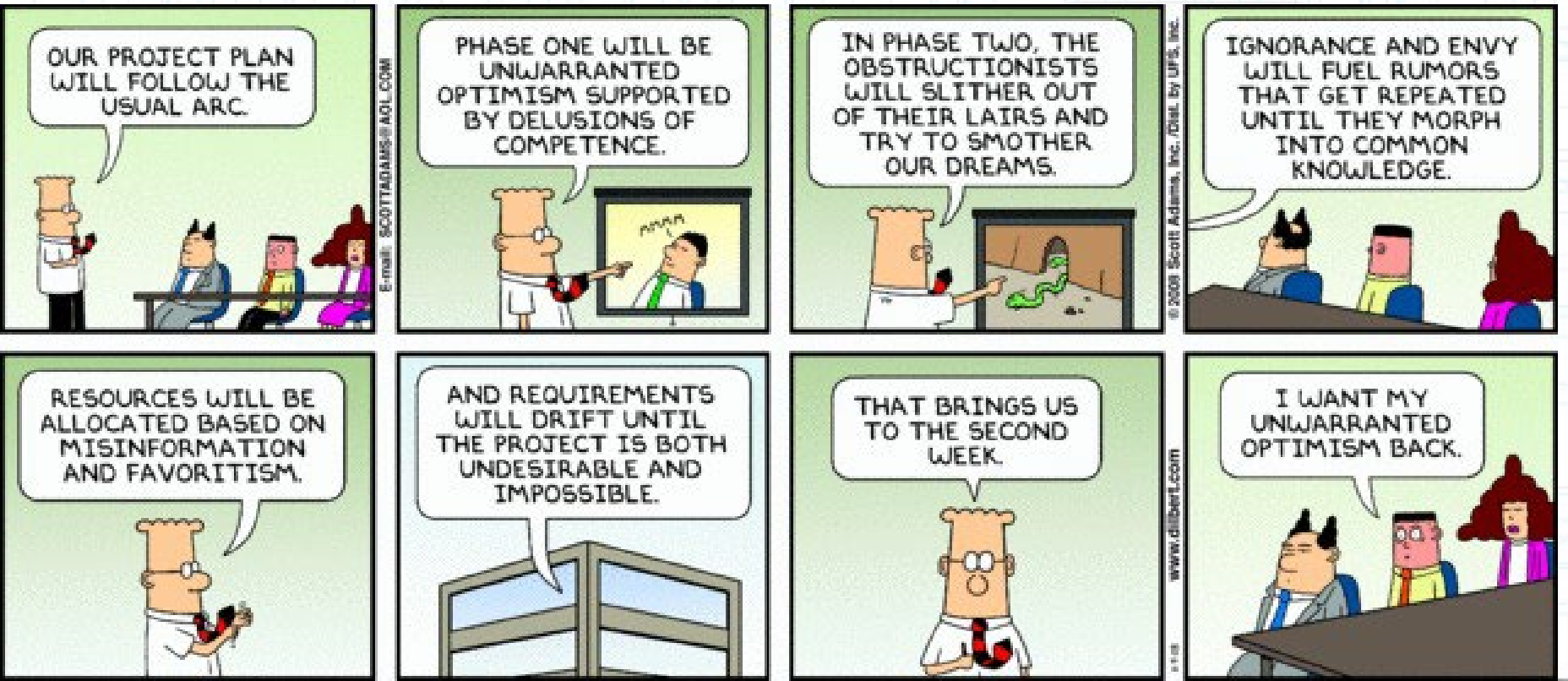
Results

- Focused on interfacing a serial temperature sensor:
  - Design approach is similar for control of other onboard components



Conclusion

- FPGA's are complicated
- Xilinx Development tools are 'buggy'
- Obscure error messages



Acknowledgments

- My Mentors
  - Dr. Frank Lind
  - Dr. Phil Erickson
- Special thanks
  - Ching Lue
  - K.T. Paul
- The MIT Haystack Community
- NSF
- My Peers